Amendments to the Drawings:

The attached replacement drawing sheet makes changes to Figs. 1A and 1B, and replace the original sheet with Figs. 1A and 1B.

Attachment: Replacement Sheet

REMARKS

Claims 1-8 and 17-21 are pending in this application. By this Amendment, new claim 21 is added, and claims 9-16 are canceled. New claim 21 includes the same features as claim 9, written in independent form. No new matter is added. In view of at least the following remarks, reconsideration and allowance are respectfully requested.

The courtesies extended to Applicants' representative by Examiner Britt during the telephone interview conducted on June 21 are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below and constitute Applicants' record of the interview.

The Office Action objects to Figs. 1A and 1B as illustrating old matter. The objections to the drawings are obviated by the amendment to Figs. 1A and 1B shown in the attached Replacement Sheet.

The Office Action objects to claims 9-13 as being in improper dependent form. The objections to the claims are obviated by the above amendments.

The Office Action rejects claims 9-16 under 35 U.S.C. §112, second paragraph, as being indefinite. Here also, the 35 U.S.C. §112 rejections are obviated by the above amendments.

The Office Action rejects claims 1-8 and 17-20 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,940,414 to Takano et al. ("Takano"). This rejection is respectfully traversed.

As discussed during the interview, Takano fails to disclose at least a second selector having "a second input to which an output signal from the second macro block is input," as recited in independent claim 1. Referring to Fig. 2 of Takano, it is apparent that multiplexer MUX1 is connected to an output terminal of circuit block A, and multiplexer MUX2 is provided between external input terminal EXT11 and an input terminal of circuit block B.

See, also, Takano at col. 4, lines 29-40. Takano does not describe any embodiments where a second selector includes an input to which an output signal from the second macro block is input.

As Applicants also discussed with the Examiner during the interview, Takano fails to disclose the first and second test modes recited in independent claim 1. Specifically, Takano does not suggest a test circuit where, during a first test mode, "the second selector outputs to the first macro block the output signal that has been input from the first selector to the first input of the second selector," as recited in claim 1. In this regard, the second multiplexer cited in the Office Action MUX2 is not configured to output to circuit block A. In this regard, Takano teaches that during testing of circuit block A, an output signal of circuit block A is outputted through the second multiplexer MUX2 to an external output terminal EXT12. See, Takano at col. 5, lines 43-45. Takano does not describe a test circuit where the second selector outputs to the first macro block.

Takano additionally fails to disclose that, during a second test mode, the "second selector outputs the output signal from the second macro block that has been input to the second input of the second selector, as a test output signal," as recited in claim 1. As noted above, Takano does not provide any means for inputting an output signal from the second macro block. Thus, when circuit B is to be tested, Takano teaches that test signal TSTB is sent through circuit block B. See, Takano at col. 5, line 64 - col. 6, line 7. There is no indication that the output signal from circuit block B is input into the second multiplexer MUX2.

As pointed out during the interview, the foregoing points are illustrated in Figs. 3A and 3B of the pending application. As shown in Fig. 3A, the test circuit described in one embodiment of the invention is operative to detect faults in connecting portion 12 for the input to the first macro block. Similarly, in the embodiment illustrated in Fig. 3B, the test

circuit is operative to detect faults located in connecting portion 14 for the output of the second macro block. In contrast, the circuit described in Takano would be inoperable to detect defects located at a path on the input to circuit block A, or on a path on the output of circuit block B.

Independent claim 17 is directed to a method for using a test circuit having similar features to the test circuit recited in independent claim 1. Additionally, independent claim 21 is directed to an integrated circuit that includes a test circuit having similar features to those referred to in claim 1. Accordingly, for at least the above reasons, claims 1, 17 and 21 are patentable over Takano.

Claims 2-8 and 18-20 depend from one of independent claims 1 and 17, and are therefore patentable over Takano for at least the reasons enumerated above, as well as for the additional features they recite.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-8 and 17-21 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Aaron L. Webb
Registration No. 56,930

JAO:ALW/gml

Attachment:
Replacement Sheet

Date: June 22, 2007

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our
Deposit Account No. 15-0461